

On Page 6, replace the paragraph beginning at line 3 with the following re-written paragraph:

#### 1.1 Integrated Circuit Connection Circuitry

Busses 60b, 62b, 64b, 72 and the first through third SEL lines 60a, 62a, 64a provide a plurality of internal connections within the ~~ASIC~~ASIC chip that comprises system controller 30 and may be referred to as such. The host bus 22, memory bus 42 and I/O bus 54 provide a plurality of external inputs and outputs for the ASIC chip that comprises the system controller 30. These inputs and outputs may be implemented in the form of leads from the packaging for the chip. The packaging may be a dual-in-line (DIP) package, pin-in-hole package, leadless ceramic package, gull-wing or j-lead package, pin-grid array package, ball grid array, plastic ball grid array or EGA enhanced.